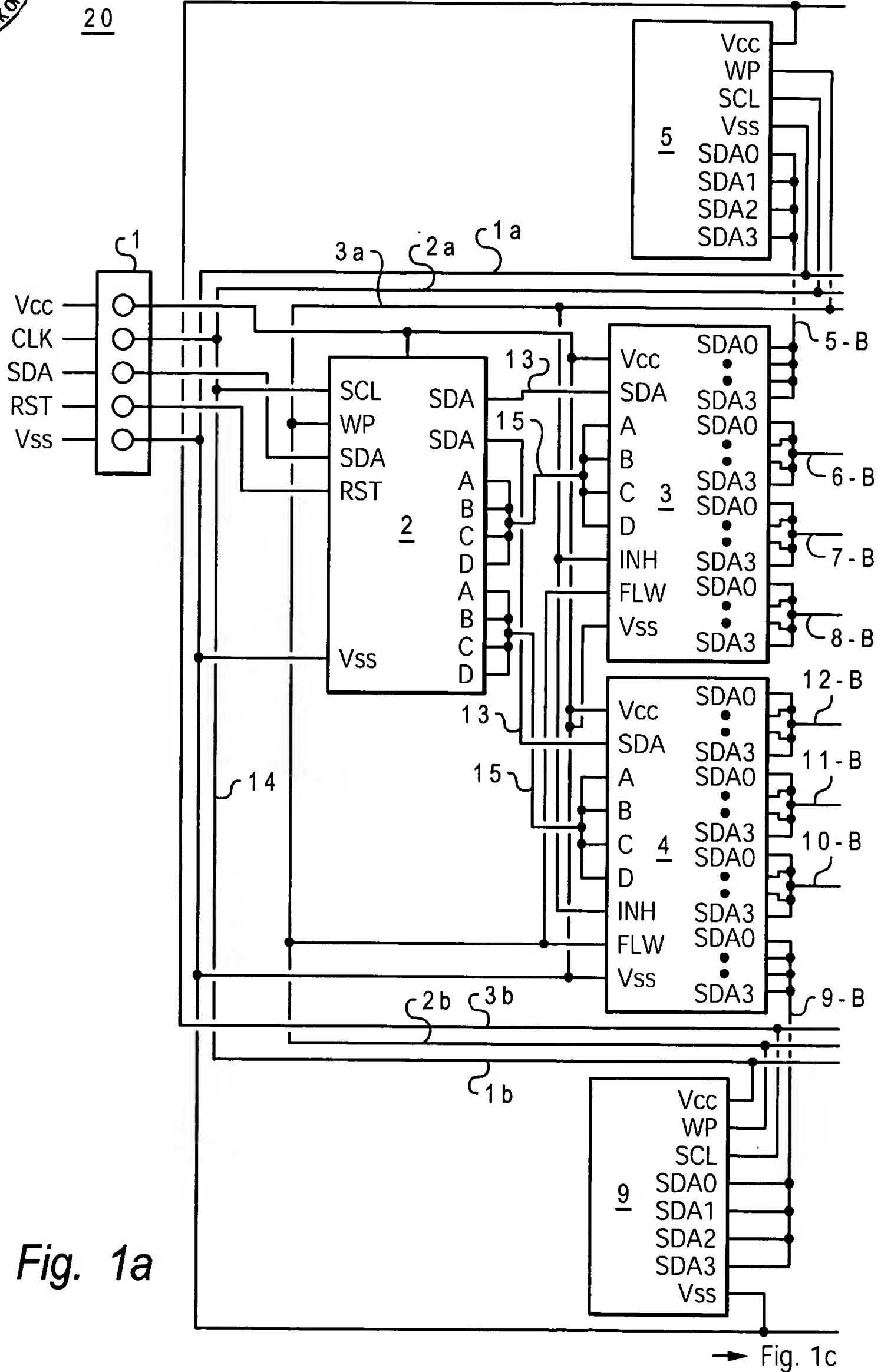


BGC002

1/15

→ Fig. 1b





BGC002

2/15

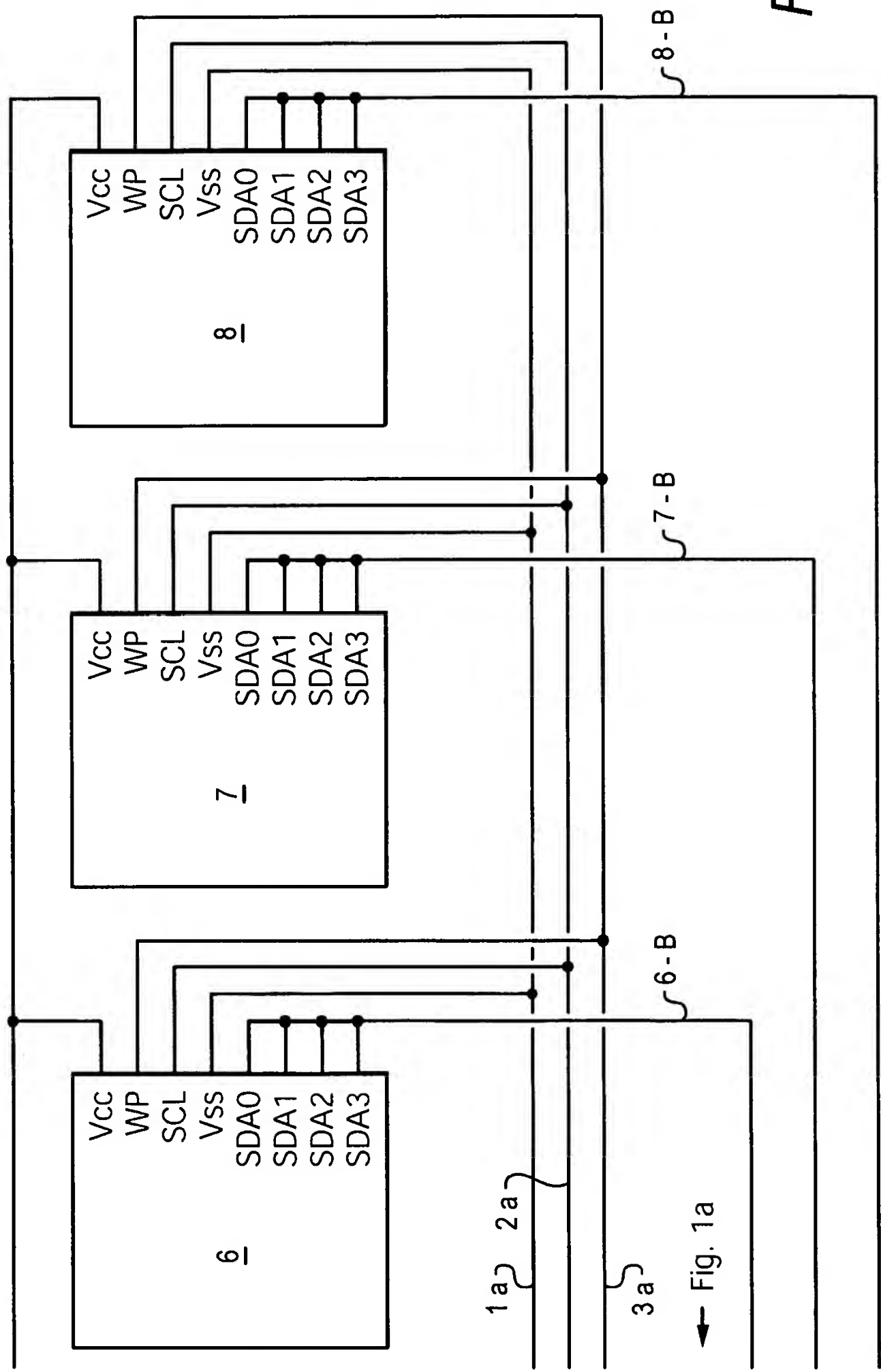
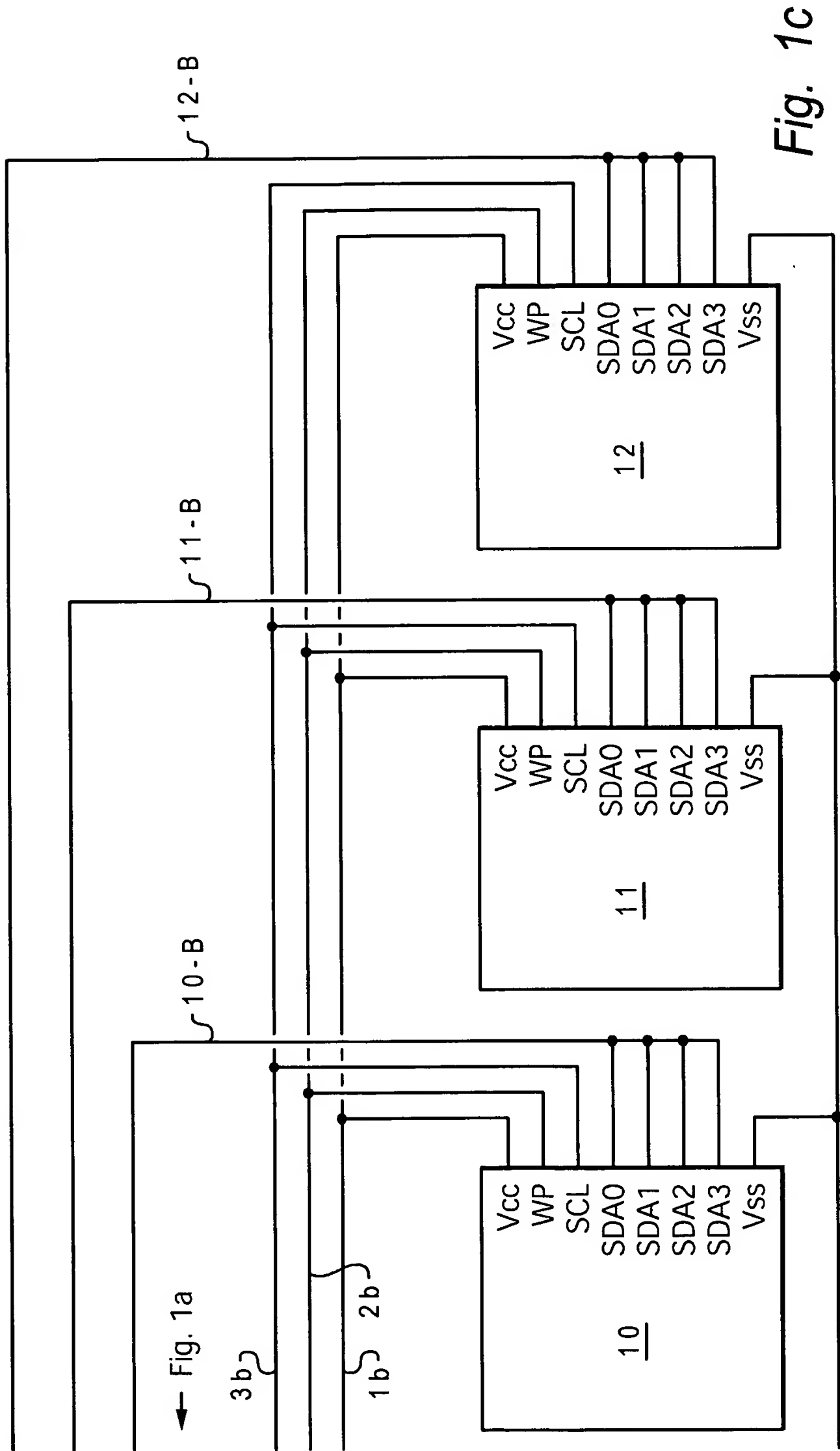


Fig. 1b



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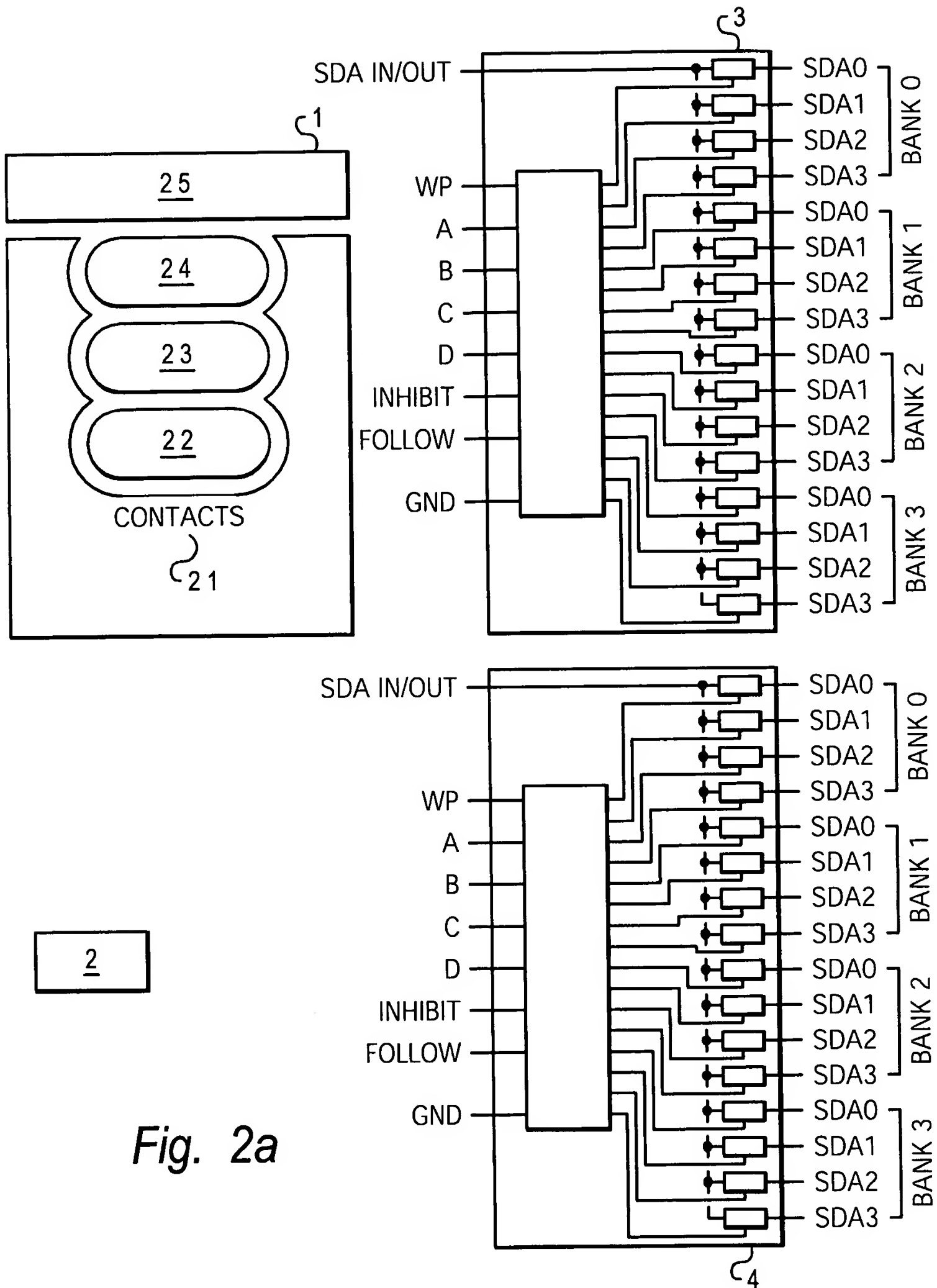
3/15





BGC002

4/15

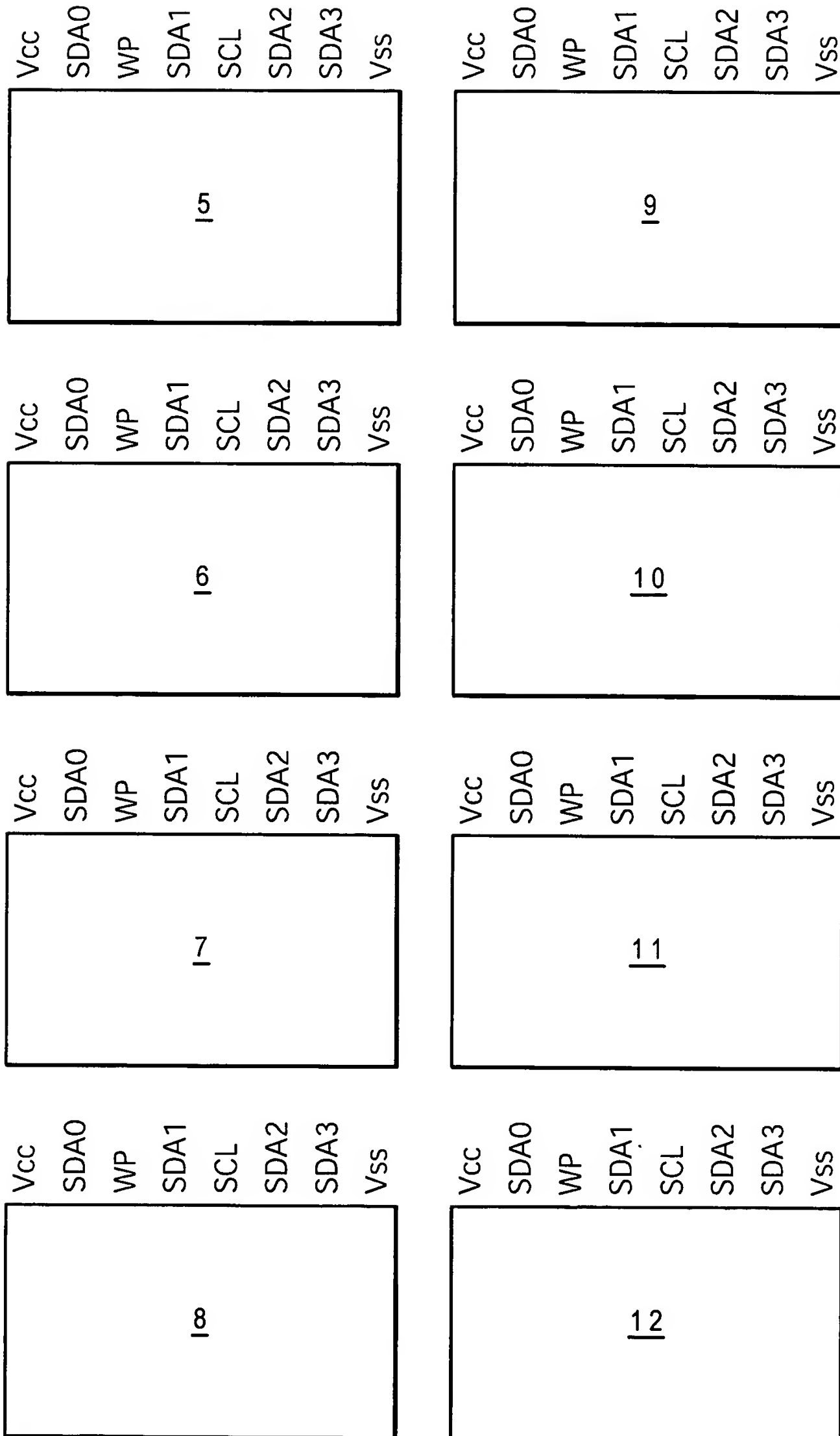




BGC002

5/15

*Fig. 2b*





BGC002

6/15

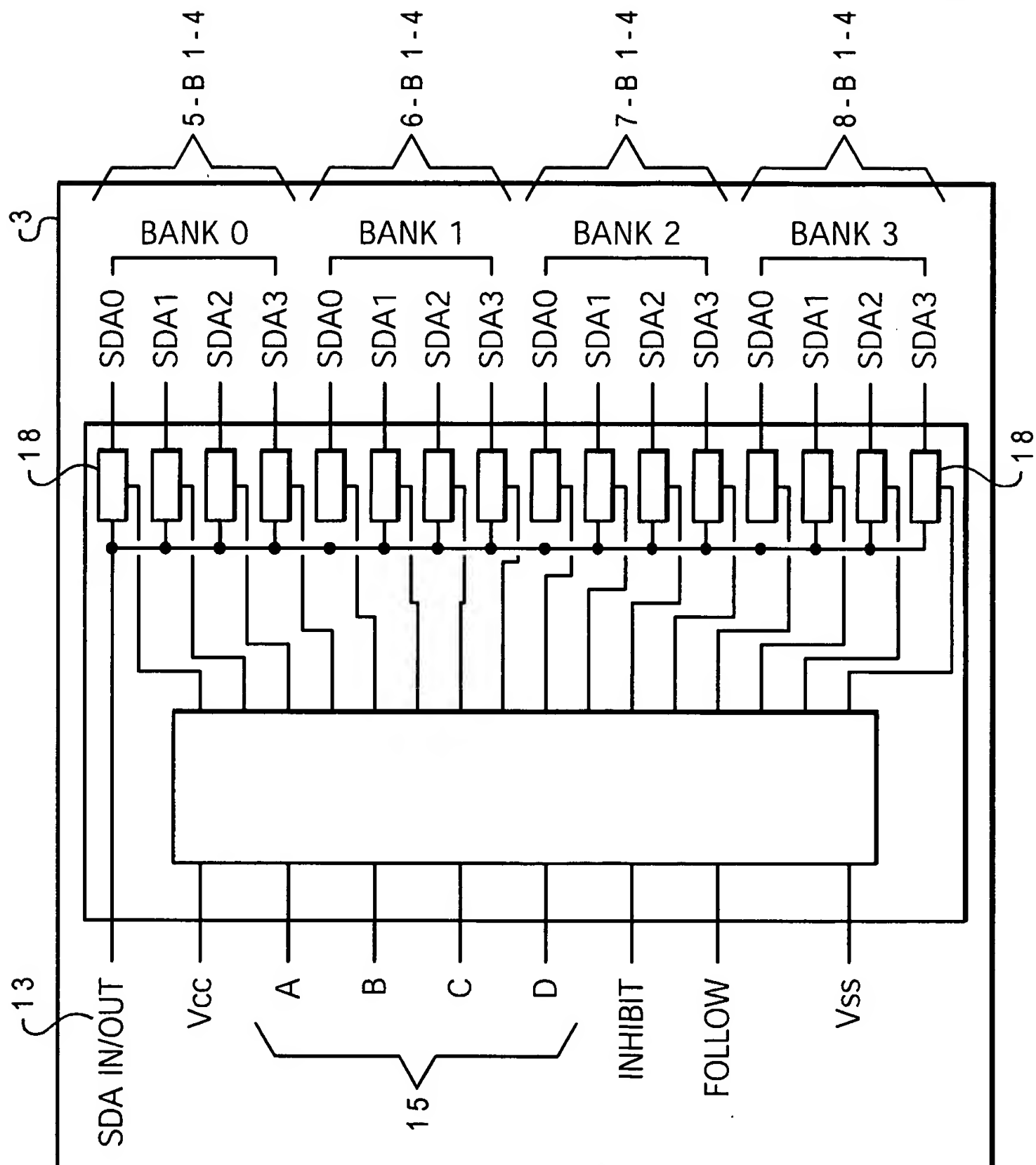


Fig. 3



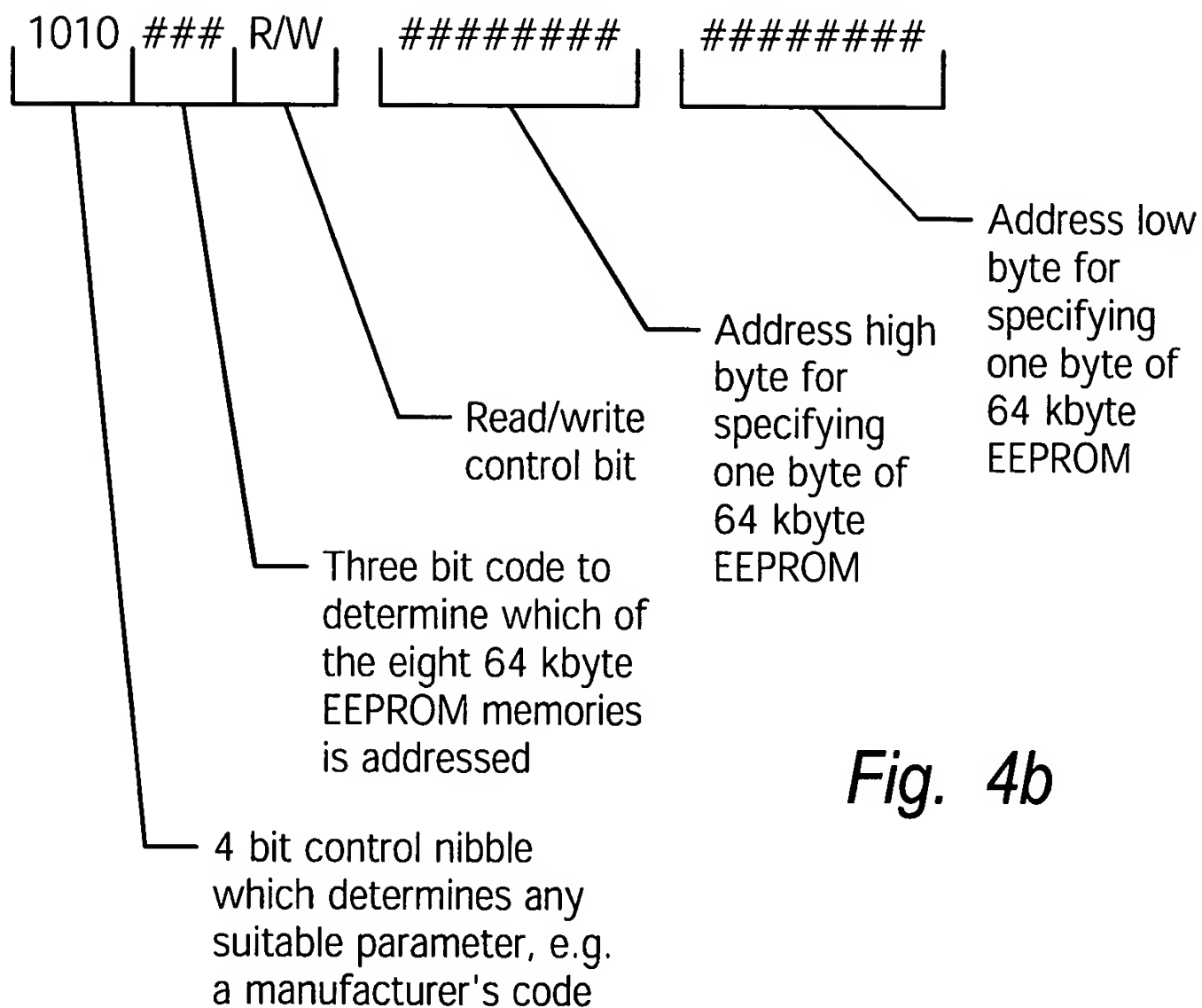
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7/15

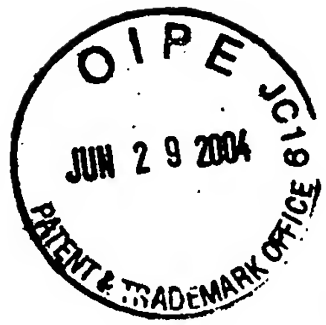


4 bit parallel address portion defines one of the serial outputs of the dispatcher. Each serial output is connected to one memory unit.

*Fig. 4a*



*Fig. 4b*



BGC002

8/15

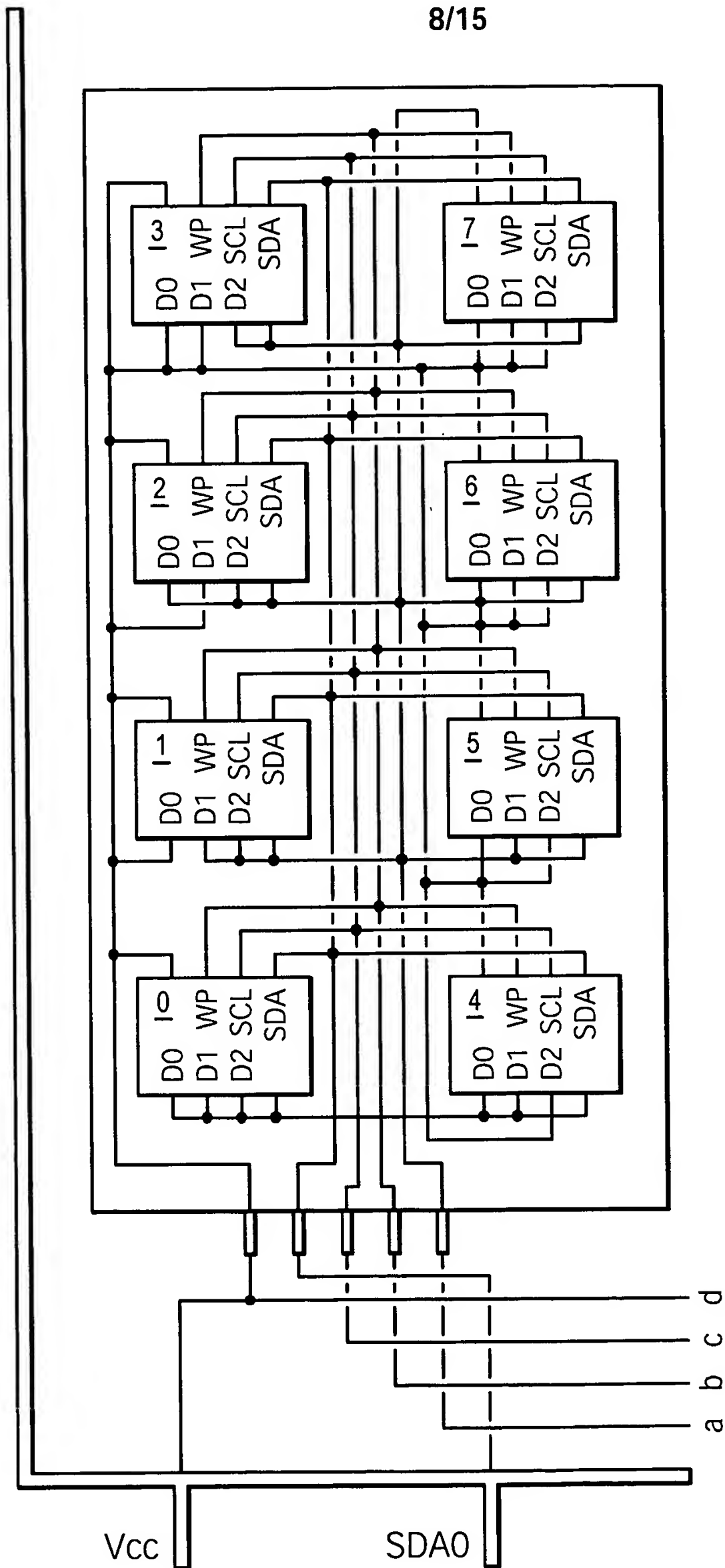


Fig. 5a

→ Fig. 5b



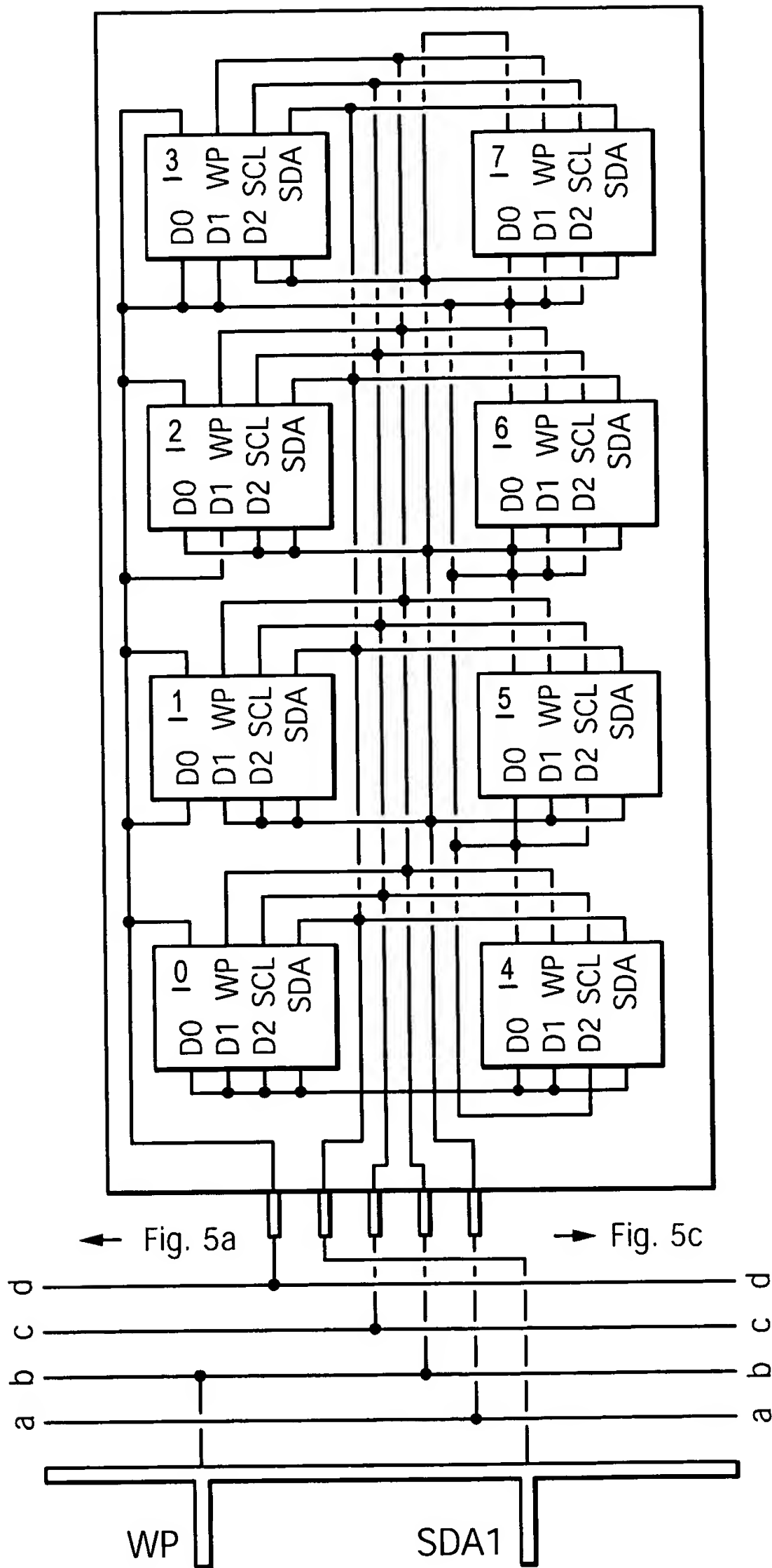


Fig. 5b



BGC002

10/15

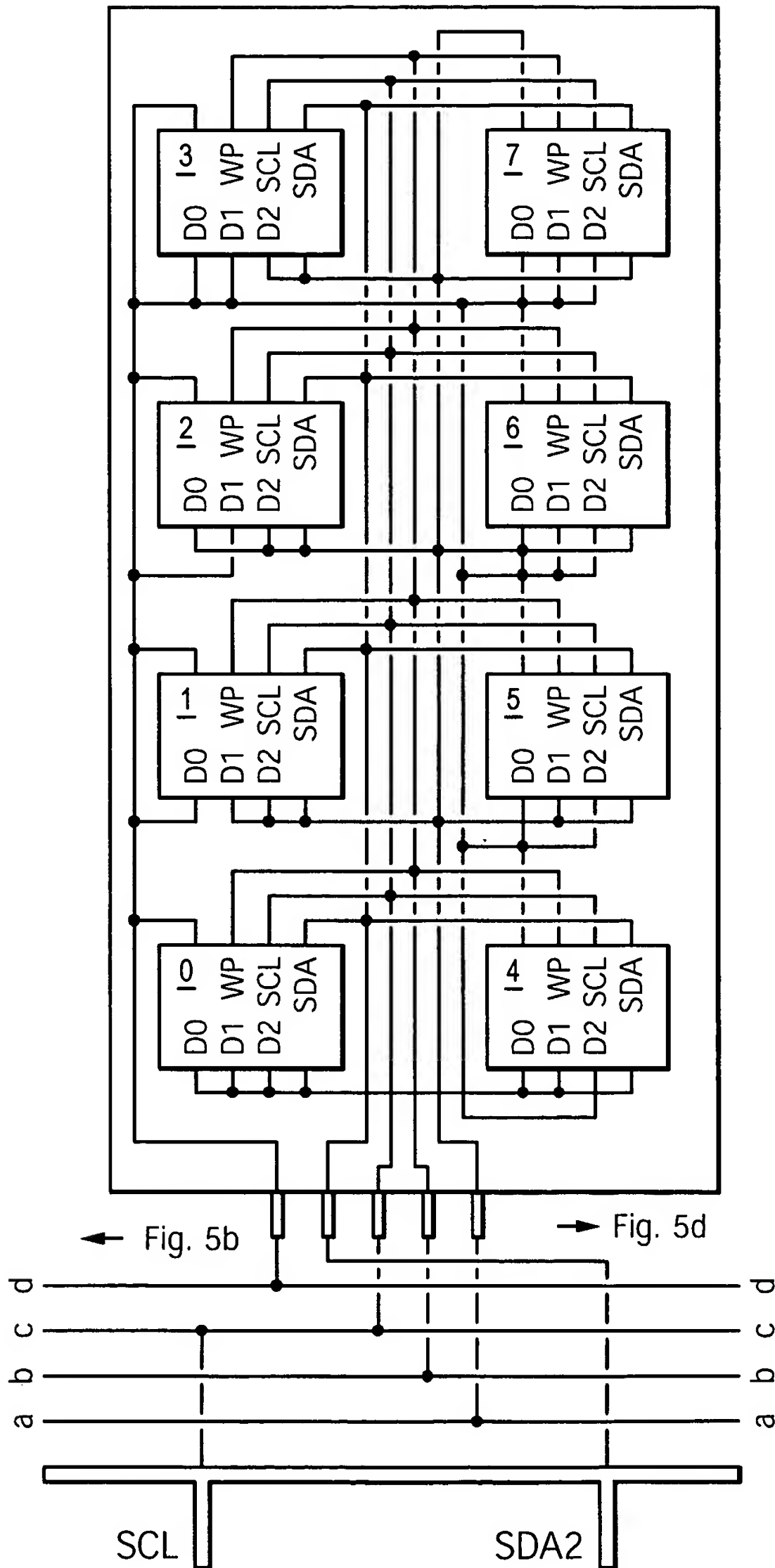


Fig. 5c

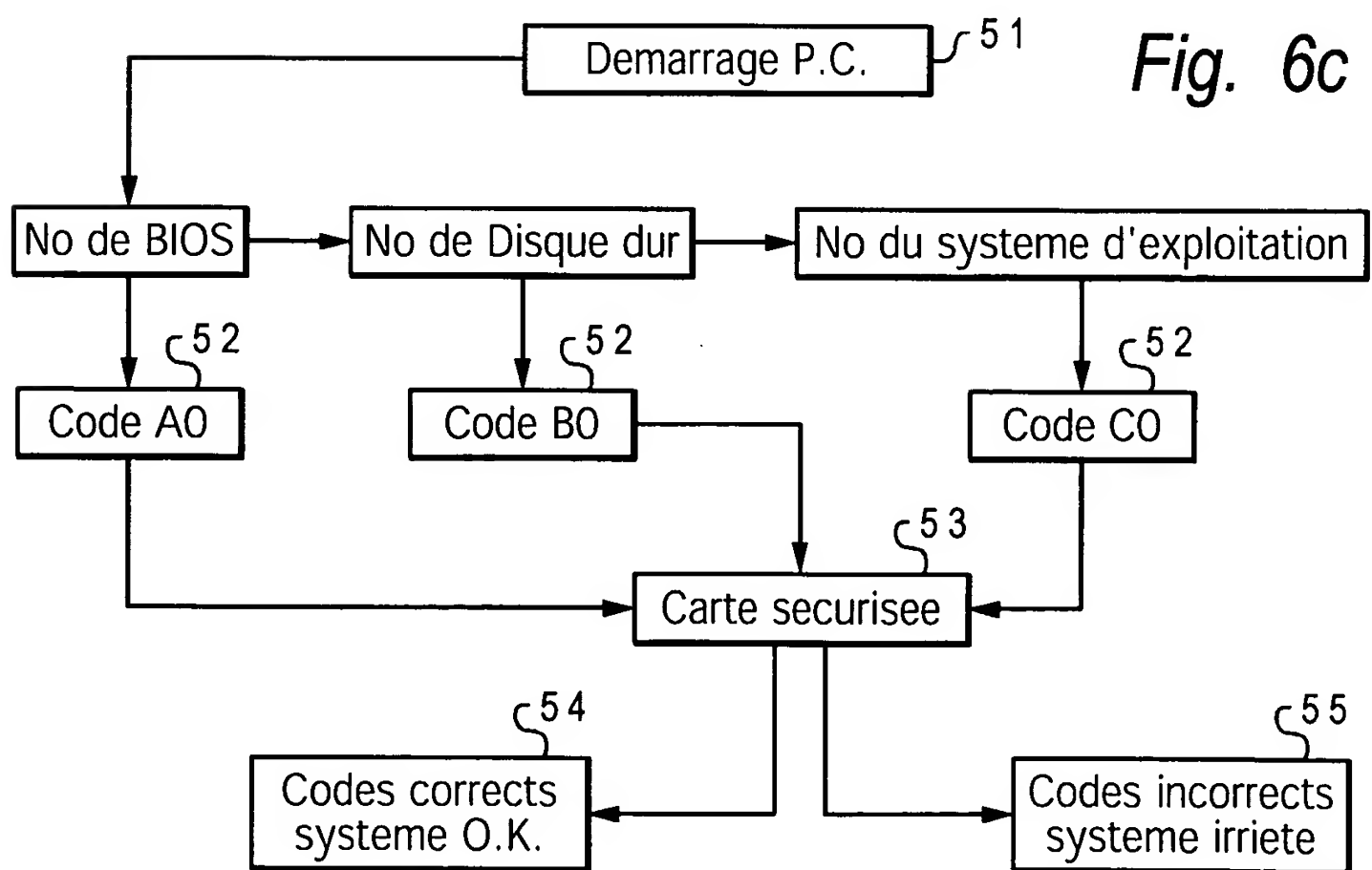
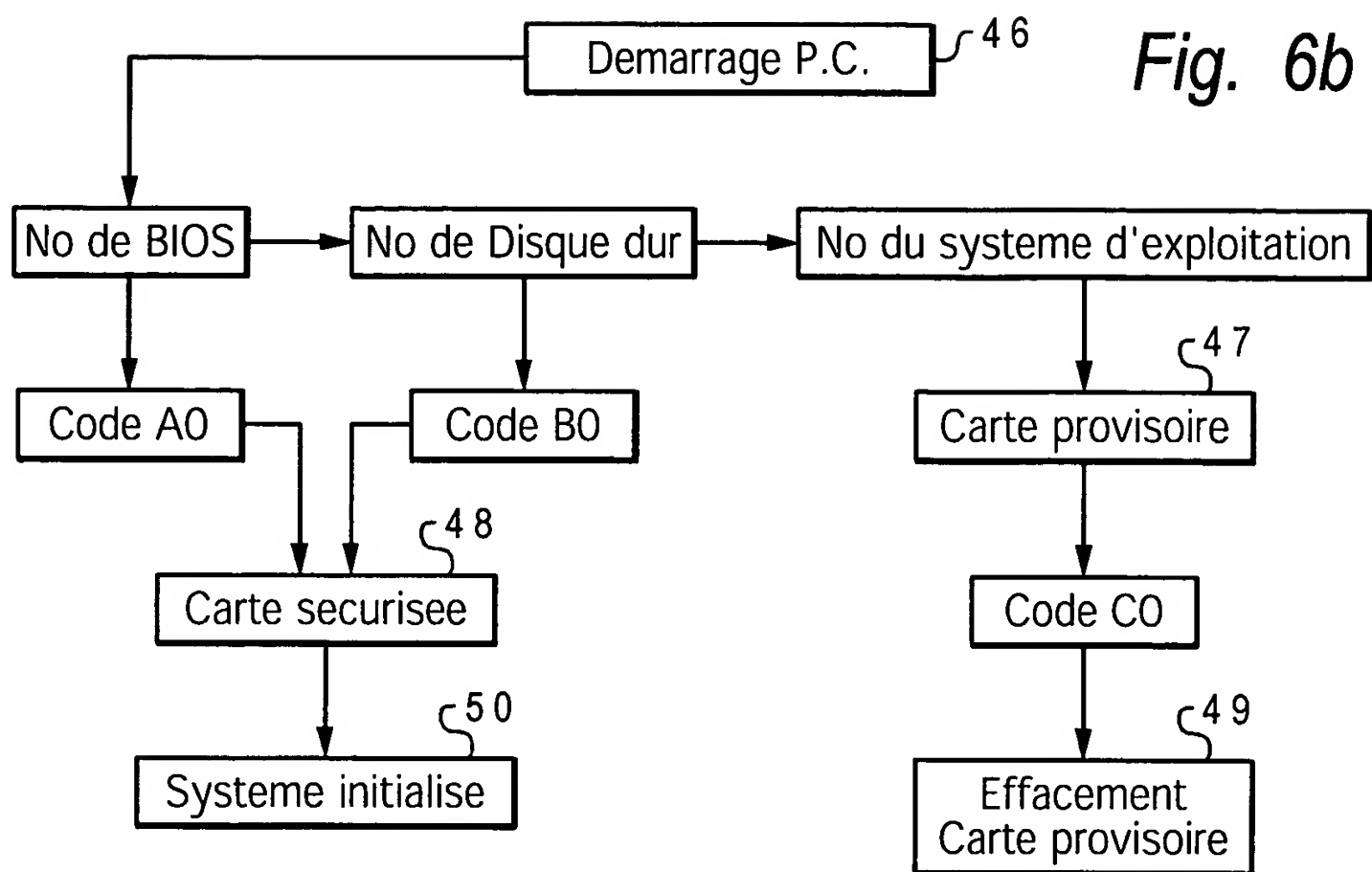
[illegible]





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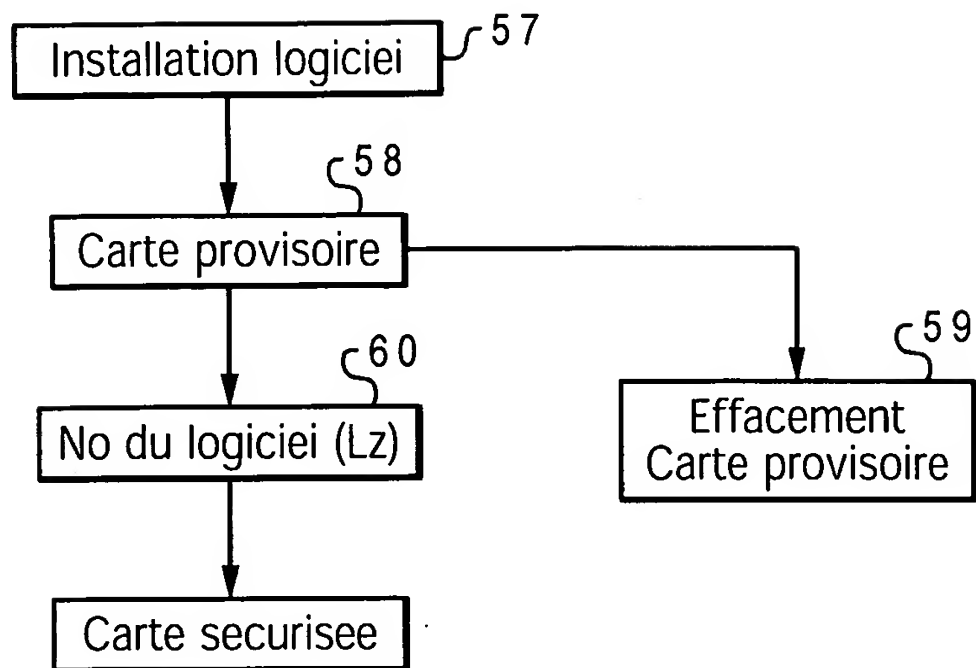
13/15



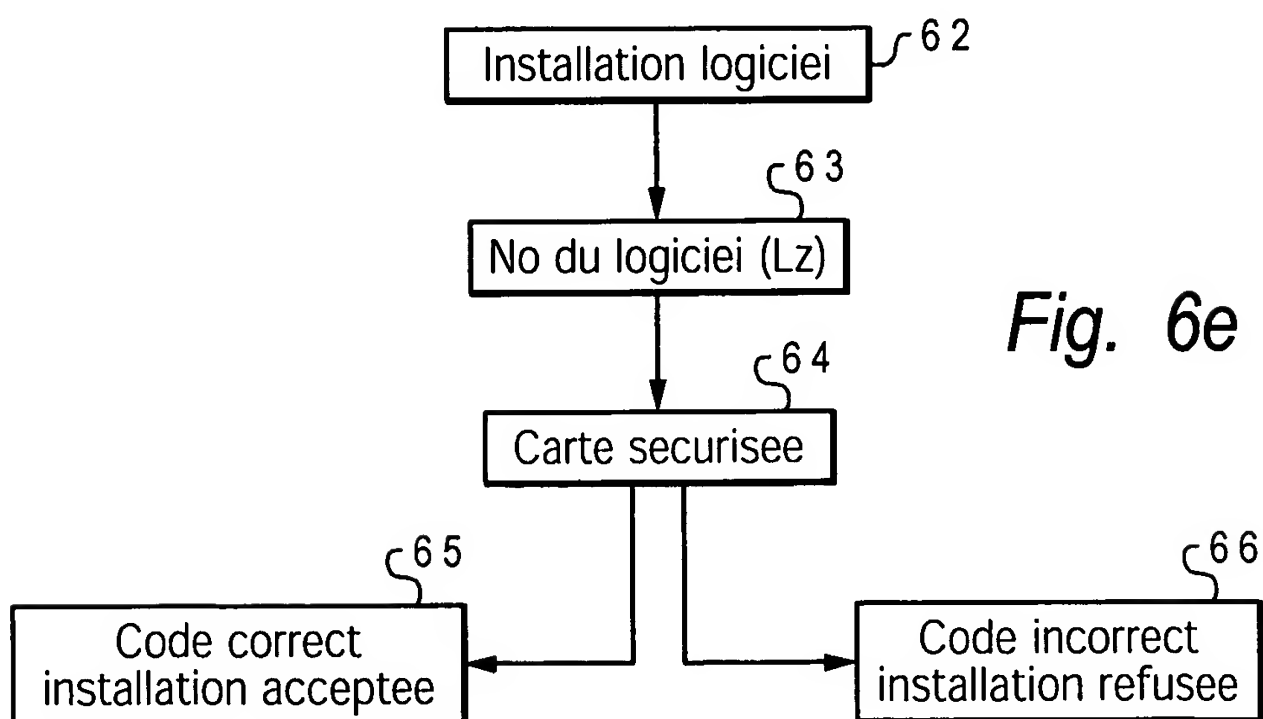


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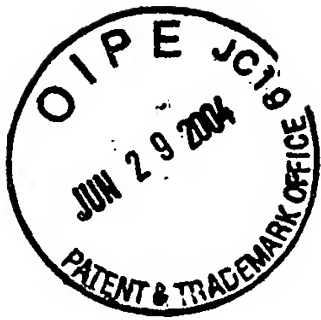
14/15



*Fig. 6d*

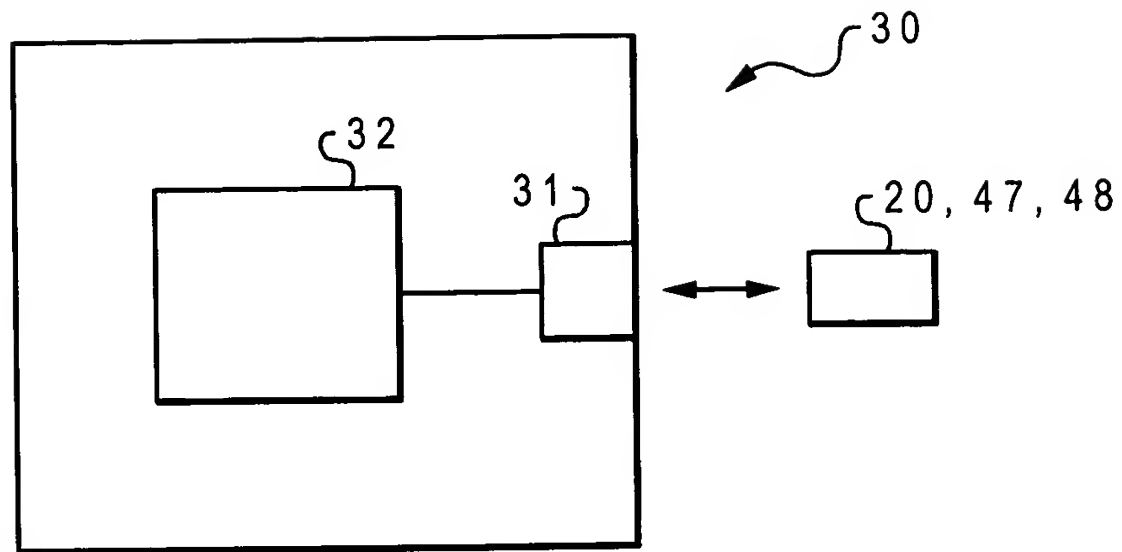


*Fig. 6e*

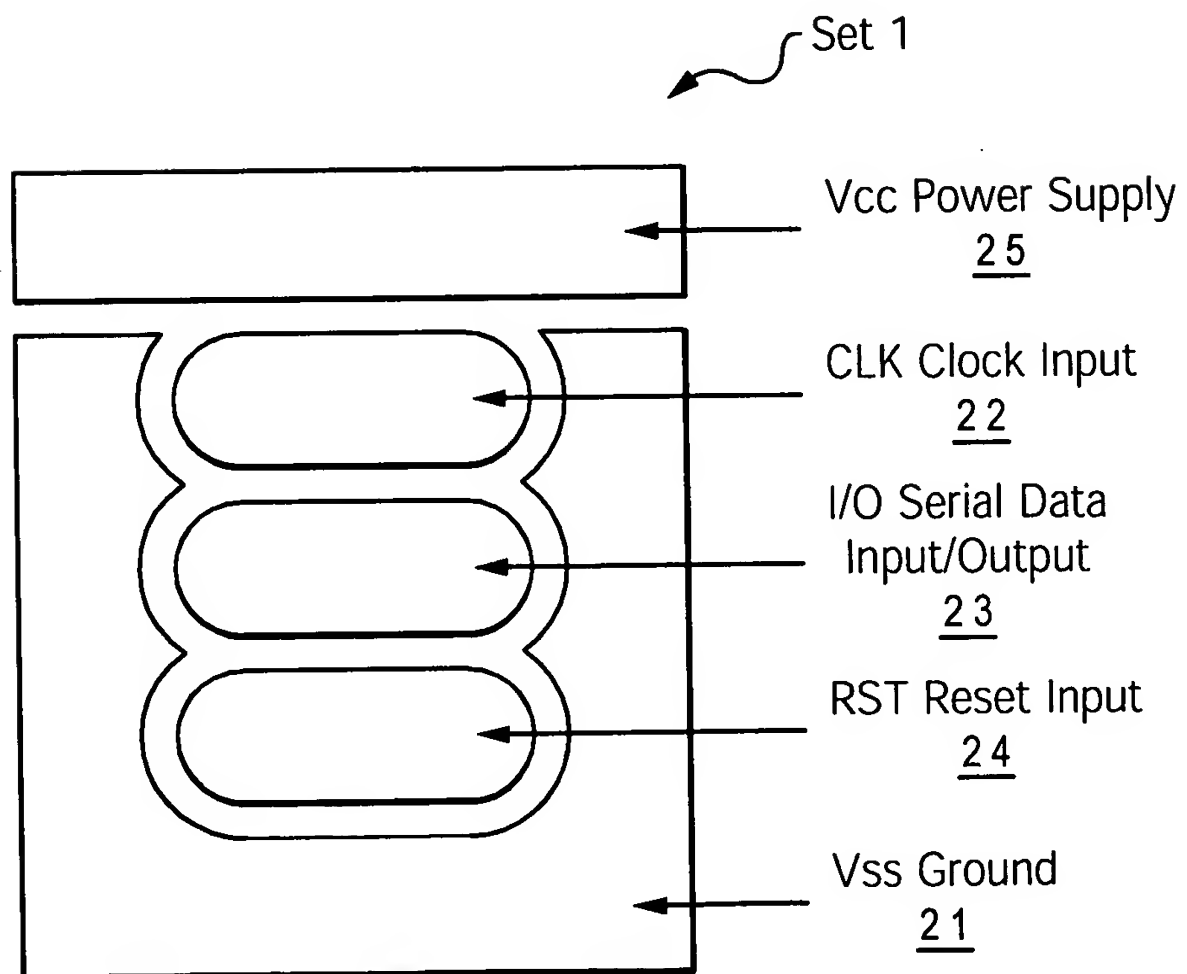


BGC002

15/15



*Fig. 7*



*Fig. 8*